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EXAMINER	
GUILL, RUSSELL L	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/994,574	WHEELER ET AL.	
	Examiner	Art Unit	
	Russ Guill	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-7,10-13,15,18,21-23 and 25-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-7,10-13,15,18,21-23 and 25-27* is/are rejected.

7)☒ Claim(s) *1* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to an Amendment filed May 4, 2007. No claims were added or cancelled. Claims 1, 4 – 7, 10 – 13, 15, 18, 21 – 23 and 25 - 27 are pending. Claims 1, 4 – 7, 10 – 13, 15, 18, 21 – 23 and 25 - 27 have been examined. Claims 1, 4 – 7, 10 – 13, 15, 18, 21 – 23 and 25 - 27 have been rejected.

2. **As previously recited, the Examiner would like to thank the Applicant for the well-presented response, which was useful in the examination process.** The Examiner appreciates the effort to perform a thorough analysis and make appropriate arguments and amendments.

3. This Office Action is NON-final.

Response to Arguments

4. Regarding **claims 1, 7, 15 and 18** rejected under 35 U.S.C. § 101:

4.1. Applicant's arguments have been fully considered, but are not persuasive for **claims 1 and 15**, as follows. However, the rejections are withdrawn, and replaced with an objection for claim 1, and a rejection under 35 USC § 112, second paragraph, for claim 15.

4.2. Applicant's arguments have been fully considered, and are persuasive for **claims 7 and 18**. Accordingly, the rejections are withdrawn.

4.3. Regarding claim 1, the Applicant argues:

4.4. In the action mailed January 5, 2007, claim 1 was rejected under 35 U.S.C. § 101 as allegedly being directed to nonstatutory subject matter. As best understood by Applicant, the rejection contends that a system that includes a database and a logic design module is an abstract idea. *See Office action mailed* January 5, *2007*, page 6, para. 9.1. The rejection also contends that a logic design module must actually perform operations to constitute patentable subject matter.

4.5. As a threshold matter, Applicant would like to point out that nothing requires the logic design module recited in claim 1 to be implemented exclusively as software, as appears to be contended in the rejection. For example, the logic design module can be implemented as hardware.

4.6. Turning to the rejection, the contention that a system *is* abstract solely because it potentially includes software defies logic. The Examiner is invited to consider the systems around him that potentially include software such as, e.g., motor vehicles, watches, cell-phones, and the like. A contention that these systems are abstract solely because they potentially include software is simply illogical. Moreover, to the best of applicant's knowledge, no judicial exception to the indication in 35 U.S.C. § 101 that machines, manufactures, and improvements thereto constitute patentable subject matter has ever been made on the basis of potentially including software.

4.7. Also, the contention that a logic design module is an abstract idea is also without basis. Instead, a logic design module (even if implemented in software) produces concrete, useful, and tangible

results, much like word processors or web browsers that are implemented in software. In particular, logic design modules produce logic designs. Logic designs have clear utility in designing logic—which is clearly a concrete, useful, and tangible result.

4.8. As for the contention that a logic design module must actually perform operations to constitute patentable subject matter, Applicant respectfully disagrees. The requirements of 35 U.S.C. § 101 simply do not require claims to recite the actual performance of operations. For example, claims directed to a hammer need not recite that the hammer is actually driving a nail. Claims directed to a car need not recite that the car is actually driving down the road. Similarly, applicant submits that claims to a logic design module need not recite that the logic design module is actually updating a logic design or indicating design discrepancies.

4.9. Accordingly, claim 1 and the claims dependent therefrom are directed to patentable subject matter. Applicant respectfully requests that the rejections of claim 1 and the claims dependent therefrom be withdrawn.

4.9.1. The Examiner respectfully replies:

4.9.2. The rejection does not assert that the system is abstract, rather, the rejection asserts that the claim includes an abstract idea. If a claim includes an abstract idea, then the claim must be directed to a practical application of the abstract idea (MPEP 2106, section IV DETERMINE WHETHER THE CLAIMED INVENTION COMPLIES WITH 35 U.S.C. 101). Further, software that performs data manipulation is clearly a judicial exception because data manipulation is an abstract idea.

4.9.3. The specification recites that the invention may be implemented entirely in software (specification, page 9, lines 9 – 11), and therefore, the logic design module may be interpreted as entirely software. If a claim can be interpreted to be non-statutory, then the claim must be amended to have only a statutory interpretation. In order for a system to produce a tangible result, there must be a processor that is functionally coupled to the software in order to realize the functionality of the software.

4.9.4. The Examiner agrees that a claim directed to a hammer does not need to produce a tangible result, but a hammer does not contain a judicial exception of an abstract idea (software). Since claim 1 appears to contain an abstract idea (software), the claim must have a practical application of the abstract idea.

4.10. Regarding claim 7, the Applicant argues:

4.11. Claim 7 was rejected under 35 U.S.C. § 101 as allegedly being directed to nonstatutory subject matter. The rejection contends that updating computer code and indicating design discrepancies is not a tangible result.

4.12. Applicant respectfully disagrees. Members of an entire profession (i.e., computer programmers) spend their days updating computer code. Applicants submit that the fruits of their labor are tangible enough to meet the requirements of any judicial exception to 35 U.S.C. § 101. Similarly, design

discrepancies prevent logic designs from operating as intended. Indicating such design discrepancies automatically is clearly a tangible result, since information needed for the proper operation of a logic design is a tangible result.

4.13. Accordingly, claim 7 and the claims dependent therefrom are directed to patentable subject matter. Applicant respectfully requests that the rejections of claim 7 and the claims dependent therefrom be withdrawn.

4.13.1. The Examiner respectfully replies:

4.13.2. Applicant's arguments are persuasive. More likely than not, the claim produces a tangible result.

4.14. Regarding claim 15, the Applicant argues:

4.15. Claim 15 was rejected under 35 U.S.C. § 101 as allegedly being directed to nonstatutory subject matter. As best understood by Applicant, the rejection contends that an apparatus that includes a central database, modification logic, and an interface could potentially be non-statutory subject matter on the ground that the apparatus is able to "perform abstract operations, such as changing a bit width." *See Office action mailed January 5, 2007,* page 6, para. 9.3. The rejection is also understood to contend that the recited "modification logic" is non-statutory subject matter for not reciting a processor.

4.16. As a threshold matter, Applicant would like to point out that nothing requires the modification logic recited in claim 15 to be implemented exclusively as software, as appears to be contended in the rejection. For example, the modification logic can be implemented as hardware.

4.17. Turning to the rejection, the contention that a system is not patentable subject matter simply because it has the ability to perform abstract operations has never been recognized as an exception to the patentable subject matter defined under 35 U.S.C. § 101. Accordingly, the rejection is improper.

4.18. Moreover, the contention that "modification logic" is non-statutory subject matter for not reciting a processor is also without basis. As discussed above, nothing requires the modification logic recited in claim 15 to be implemented exclusively as software. Further, the mere fact that a claim recites logic absent a processor has never been recognized as an exception to the patentable subject matter defined under 35 U.S.C. § 101. Accordingly, the basis of the rejection is improper.

4.19. Accordingly, claim 15 and the claims dependent therefrom are directed to patentable subject matter. Applicant respectfully requests that the rejections of claim 15 and the claims dependent therefrom be withdrawn.

4.19.1. The Examiner respectfully replies:

4.19.2. If a claim includes an abstract idea, then the claim must be directed to a practical application of the abstract idea (MPEP 2106, section IV DETERMINE WHETHER THE CLAIMED INVENTION COMPLIES WITH 35 U.S.C. 101). The claim does not appear to produce a tangible

result to support a practical application, and the Applicant does not appear to have addressed the missing tangible result.

4.19.3. The specification recites that the invention may be implemented entirely in software (specification, page 9, lines 9 - 11), and therefore, the modification logic and interface may be interpreted as entirely software. If a claim can be interpreted to be non-statutory, then the claim must be amended to have only a statutory interpretation. In order for an apparatus to produce a tangible result, there must be a processor that is functionally coupled to the software in order to realize the functionality of the software.

4.20. Regarding claim 18, the Applicant argues:

4.21. Claim 18 was rejected under 35 U.S.C. § 101 as allegedly being directed to nonstatutory subject matter. As best understood by Applicant, the rejection contends that the recited machine-accessible medium "appears to contain abstract operations." *See Office action mailed January 5, 2007,* page 6, para. 9.4. The rejection also contends that updating computer code and indicating design discrepancies is not a tangible result.

4.22. Applicant respectfully disagrees. As for the machine-accessible medium containing abstract operations, claim 18 recites a machine-accessible medium that contains instructions which cause a machine to perform operations. Machine-accessible media that contain instructions are clearly tangible and within the scope of 35 U.S.C. § 101.

4.23. As for the contention that updating computer code and indicating design discrepancies is not a tangible result, as discussed above, both of these activities are clearly tangible enough to meet the requirements of 35 U.S.C. § 101.

4.24. Accordingly, claim 18 and the claims dependent therefrom are directed to patentable subject matter. Applicant respectfully requests that the rejections of claim 15 and the claims dependent therefrom be withdrawn.

4.24.1. The Examiner respectfully replies:

4.24.2. Applicant's arguments are persuasive. More likely than not, the claim produces a tangible result.

5. Regarding **claims** rejected under 35 U.S.C. § 103:

5.1. Applicants' arguments have been fully considered, and are persuasive. However, after further consideration and search, new rejections are made below.

Claim Objections

6. Claim 1 is objected to for the following informalities: the claim recites in line 2, "a logic design module" that appears to be a software module. The specification recites that the invention may be implemented entirely in software (specification, page 9, lines 9 - 11), and therefore, the logic design module may be interpreted as entirely software. A system requires a processing element functionally connected to software in order to realize the functionality of a software module. Appropriate correction is required.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. **Claim 15** is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

8.1. Regarding claim 15, while a central database appears to be tangible, it is unclear whether the remaining elements are hardware, software, or some combination. Therefore, the metes and bounds of the claim cannot be determined. For the purpose of claim examination, all limitations except the central database are interpreted as software. This interpretation appears to be consistent with the specification, which recites that the invention may be implemented entirely in software (page 9, lines 9 - 11). Correction or amendment is required.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

11. **Claims 1, 4 - 6, 7, 10 - 13, 18, 21 - 23** and **25 - 27** are rejected under 35 U.S.C. 103(a) as being unpatentable over Panchul (U.S. Patent Number 6,226,776) in view of Yamagishi (Yamagishi, Kunihiko; Sekine, Masatoshi; A multi-representational design data capture system, 1993, IEEE 1993 Custom Integrated circuits conference), further in view of IEEE Verilog (IEEE Standard Hardware Description Language Based on the Verilog® Hardware Description Language, 1995, IEEE).

11.1. The art of Panchul is directed to a computer aided hardware design system ***(Abstract)***.

11.2. The art of Yamagishi is directed to logic design systems ***(page 13.2.1, Abstract, and section 1 Introduction)***.

11.3. The art of IEEEVerilog is directed to logic design ***(page iii, section Introduction)***.

11.4. The art of Panchul and the art of Yamagishi are analogous art because they are both directed to a hardware design system.

11.5. The art of Panchul and the art of IEEEVerilog are analogous art because they both contain the art of logic design.

11.6. Regarding **claim 1**:

11.7. Panchul appears to teach:

11.7.1. a logic design module operable to be used by one or more users to generate a logic design as part of an electrical circuit, wherein the logic design includes labels (*figure 18B1, it would have been obvious that a logic design module was used to build the displayed code, wherein the logic design module was a tool such as SILOS III from Simucad, or a text editor*).

11.7.2. a collection of modifiable values of signal parameters that are accessible by the logic design module, wherein the values of signal parameters are associated with the labels in the logic design (*figure 18B1, it would have been obvious that the parameters ADDRESS_SIZE and DATA_SIZE were signal parameters, and that they were accessible*).

11.7.3. The logic design module is operable to update the logic design to reflect modification of the values of the signal parameters by modifying the logic design to be compatible with the modified values of the signal parameters (*figure 18B1, it would have been obvious that compiling the Verilog code would have used the signal parameters to modify the signal widths, such as out_data, to be compatible with the modified values of the signal parameters*).

11.8. Panchul does not specifically teach:

11.8.1. *a central database integrated with the logic design module*.

11.8.2. The logic design module is operable to update the logic design to reflect modification of the signal parameters *in the central database*.

11.8.3. to indicate design discrepancies in the logic design resulting from the modifications to the values of the signal parameters in the central database automatically.

11.9. Yamagishi appears to teach:

11.9.1. a central database integrated with the logic design module ***(pages 13.2.2 and 13.2.3, section 2.2 Database FALNET)***.

11.10. IEEEVerilog appears to teach:

11.10.1. to indicate design discrepancies in the logic design resulting from the modifications to the values of the signal parameters in the central database automatically (***page 59, lines 1 – 25***).

11.10.1.1. Regarding (***page 59, lines 1 – 25***); it would have been obvious that updating a signal bit width incorrectly for terminal connections would result in too few or too many bits to connect all the instances, which would cause an error.

11.11. The motivation to use the art of Yamagishi with the art of Panchul would have been obvious given the statement in Yamagishi that the database allows much closer integration among tools than other commercially available frameworks ***(page 13.2.3, left-side of page, lines 1 – 3)***, which would have been recognized as a benefit by the ordinary artisan.

11.12. The motivation to use the art of IEEEVerilog with the art of Panchul would have been the knowledge of the ordinary artisan that indicating design discrepancies would save time and effort by allowing the ordinary artisan to correct the discrepancies and thereby make the logic design functional.

11.13. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Yamagishi and the art of IEEEVerilog with the art of Panchul to produce the claimed invention.

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11.14. Regarding **claim 4**:

11.15. Panchul appears to teach indicating a bit width (*figure 18B1, input signal in_unit has a bit width)*.

11.16. Panchul does not specifically teach indicating a bit width *error*.

11.17. IEEEVerilog appears to teach indicating a bit width error (*page 59, lines 1 - 25)*.

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11.18. Regarding **claim 5**:

11.19. Panchul appears to teach:

11.19.1. the signal parameters characterize a signal bit width (*figure 18B1, input signal in_data, DATA_SIZE*).

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11.20. Regarding **claim 6**:

11.21. Panchul appears to teach:

11.21.1. the signal parameters characterize a signal bit position (*figure 18B1, input signal in_data, element [DATA_SIZE - 1 : 0]*).

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11.22. Regarding **claim 26**:

11.23. Panchul appears to teach:

11.23.1. the signal parameters define characteristics that characterize multiple bits of a multiple bit signal (*figure 18B1, input signal in_data, element [DATA_SIZE - 1 : 0]*).

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11.24. Regarding **claim 27**:

11.25. Panchul appears to teach:

11.25.1. the signal parameter defines a characteristic that characterizes multiple bits of a multiple bit signal (*figure 18B1, input signal in_data, element [DATA_SIZE - 1 : 0]*).

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11.26. Regarding **claim 7**:

11.27. Panchul appears to teach:

11.27.1. receiving an assignment of a value to a signal parameter *(figure 18B1; it would have been obvious that element DATA_SIZE received an assigned value)*

11.27.2. Maintaining the value of the signal parameter in association with an identifier of the signal parameter *(figure 18B1; it would have been obvious that the value of a signal parameter was maintained - for example, DATA_SIZE)*.

11.27.3. Using the identifier of the signal parameter to identify a first position in computer code for a logic design forming part of an electrical circuit *(figure 18B1, element DATA_SIZE; it would have been obvious that when the code was compiled that the Verilog compiler would use the*

identifier of the signal parameter to identify all positions in the computer code where the identifier was used).

11.27.4. Modifying the computer code at the first position to reflect the value (*figure 18B1, element DATA_SIZE; it would have been obvious that when the code was compiled that the Verilog compiler would modify the computer code at all positions to reflect the value*).

11.27.5. Using the identifier of the signal parameter to identify a second position in computer code for the logic design (*figure 18B1, element DATA_SIZE; it would have been obvious that when the code was compiled that the Verilog compiler would use the identifier of the signal parameter to identify all positions in the computer code where the identifier was used)*.

11.27.6. Receiving an updated value of the signal parameter (*figure 18B1, element DATA_SIZE; it would have been obvious to receive an updated value of the signal parameter through a logic design tool such as a text editor*).

11.27.7. Modifying the computer code at the second position to reflect the value (*figure 18B1, element DATA_SIZE; it would have been obvious that when the code was compiled that the Verilog compiler would modify the computer code at all positions to reflect the value*).

11.27.8. Updating both the first position and the second position in the computer code for the logic design to reflect the updated value of the signal parameter (*figure 18B1, element DATA_SIZE; it would have been obvious that when the code was compiled that the Verilog compiler would update all positions in the computer code for the logic design to reflect the updated value of the signal parameter*).

11.28. Panchul does not specifically teach:

11.28.1. Maintaining the defined signal value *in a central database*.

11.28.2. Using the identifier of the signal parameter maintained ***in the central database*** .

11.28.3. Receiving an updated value of the signal parameter ***in the central database***.

11.28.4. indicating design discrepancies occurring in the logic design that result from updating the value of the defined signal parameter automatically.

11.29. Yamagishi appears to teach:

11.29.1. a central database integrated with a logic design module (***pages 13.2.2 and 13.2.3, section 2.2 Database FALNET***).

11.30. IEEEVerilog appears to teach:

11.30.1. indicating design discrepancies occurring in the logic design that result from updating the value of the defined signal parameter automatically (***page 59, lines 1 – 25***).

11.30.1.1. Regarding (***page 59, lines 1 – 25***); it would have been obvious that updating a signal bit width incorrectly for terminal connections would result in too few or too many bits to connect all the instances, which would cause an error.

11.31. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Yamagishi and the art of IEEEVerilog with the art of Panchul to produce the claimed invention.

11.32. Regarding **claim 11**:

11.32.1. Panchul appears to teach:

11.32.1.1. the signal parameter characterizes a signal bit width and the value includes a value for the signal bit width (*figure 18B1, input signal in_data, element [DATA_SIZE – 1 : 0]*).

11.33. Regarding **claim 12**:

11.33.1. Panchul appears to teach:

11.33.2. the signal parameter characterizes a signal bit position and the value includes a value for the signal bit position (*figure 18B1, input signal in_data, element [DATA_SIZE – 1 : 0]*).

11.34. Regarding **claim 13**:

11.34.1. Panchul appears to teach:

11.34.2. the signal parameter characterizes a bit field and the value includes a value for the bit field (*figure 18B1, input signal in_data, element [DATA_SIZE – 1 : 0]*).

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11.35. Regarding **claim 10**:

11.35.1. Panchul does not specifically teach:

11.35.1.1. graphically indicating a bit width error.

11.35.2. Yamagishi appears to teach graphically indicating bit widths (**figure 1**).

11.35.3. Yamagishi appears to teach graphically indicating errors (**figure 1**).

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11.36. Regarding **claim 18**:

11.37. Panchul appears to teach:

11.37.1. Receiving a value of a signal parameter that characterizes multiple bits of a multiple bit signal (*figure 18B1, element DATA_SIZE; it would have been obvious that a value was received in order to have a value of the parameter*).

11.37.2. Maintaining the value of the signal parameter (*figure 18B1, element DATA_SIZE*).

11.37.3. Using the value of the signal parameter that is maintained, in computer code for a logic design forming part of an electrical circuit that includes the multiple bit signal (*figure 18B1, element DATA_SIZE*).

11.37.4. Receiving an update to the value of the signal parameter (*figure 18B1, element DATA_SIZE; it would have been obvious to receive an updated value of the signal parameter through a logic design tool such as a text editor*).

11.37.5. updating the logic design with the updated value of the signal parameter by modifying the logic design to be compatible with the updated signal parameter (*figure 18B1, element DATA_SIZE; it would have been obvious that compiling the Verilog code would have updated the logic design by modifying the logic design to be compatible with the updated signal parameter*).

11.38. Panchul does not teach specifically teach:

11.38.1. Using the defined signal parameter ***that is maintained in the central database*** in computer code for a logic design forming part of an electrical circuit.

11.38.2. Maintaining the value of signal parameter ***in a central database***.

11.38.3. Using the value of the signal parameter that is maintained ***in the central database***.

11.38.4. indicating design discrepancies occurring in the logic design that result from updating the value of the defined signal parameter automatically.

11.39. Yamagishi appears to teach:

11.39.1. Maintaining logic design data ***in a central database*** ***(page 13.2.1, section 2 FALcyber, and pages 13.2.2 and 13.2.3, section 2.2 Database FALNET)***.

11.40. IEEEVerilog appears to teach:

11.40.1. indicating design discrepancies occurring in the logic design that result from updating the value of the defined signal parameter automatically (***page 59, lines 1 – 25***).

11.41. The motivation to use the art of Yamagishi with the art of Panchul would have been obvious given the statement in Yamagishi that the database allows much closer integration among tools than other commercially available frameworks ***(page 13.2.3, left-side of page, lines 1 – 3)***, which would have been recognized as a benefit by the ordinary artisan.

11.42. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Yamagishi and the art of IEEVerilog with the art of Panchul to produce the claimed invention.

11.43. Regarding **claim 22**:

11.43.1. Panchul appears to teach:

11.43.1.1. the signal parameter characterizes a signal bit width and the value includes a value for the signal bit width (*figure 18B1, input signal in_data, element [DATA_SIZE - 1 : 0]*).

11.44. Regarding **claim 23**:

11.44.1. Panchul appears to teach:

11.44.1.1. the signal parameter characterizes a signal bit position and the value includes a value for the signal bit position (*figure 18B1, input signal in_data, element [DATA_SIZE - 1 : 0]*).

11.45. Regarding **claim 25**:

11.45.1. Panchul does not specifically teach:

11.45.1.1. permitting one or more users to access the central database.

11.45.2. Yamagishi appears to teach:

11.45.2.1. permitting one or more users to access the central database (*page 13.2.1, figure 1*).

11.46. Regarding **claim 21**:

11.46.1. Panchul does not specifically teach:

11.46.1.1. graphically indicating a bit width error.

11.46.2. Yamagishi appears to teach graphically indicating bit widths (**figure 1**).

11.47. Yamagishi appears to teach graphically indicating errors (**figure 1**).

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12. **Claim 15** is rejected under 35 U.S.C. 103(a) as being unpatentable over Panchul (U.S. Patent Number 6,226,776) in view of Yamagishi (Yamagishi, Kunihiko; Sekine, Masatoshi; A multi-representational design data capture system, 1993, IEEE 1993 Custom Integrated circuits conference).

12.1. Regarding **claim 15**:

12.2. Panchul appears to teach:

12.2.1. a collection of identifiers of one or more bit width signal parameters ***(figure 18B1, elements DATA_SIZE and ADDRESS_SIZE)***.

12.2.2. values associated with each of the identifiers of the bit width signal parameters ***figure 18B1, elements DATA_SIZE 32 and ADDRESS_SIZE 16)***.

12.2.3. modification logic to allow a user to modify the values associated with the identifiers individually (***figure 18B1; it would have been obvious that a tool such as a text editor would allow the user to modify the values associated with the identifiers***).

12.2.4. an interface to convey the identifiers and the associated values to a logic design module that uses the identifiers to identify where a logic design is to be changed and the values to change a bit width in the logic design to form part of an electrical circuit (*figure 18B1, elements DATA_SIZE and ADDRESS_SIZE; it would have been obvious that there was an interface, such as a Verilog compiler, that used the identifiers to identify where the logic design was to be changed*);

12.3. Panchul does not specifically teach:

12.3.1. *A central database accessible by one or more users.*

12.3.2. One or more signal parameters defined *in the central database*.

12.3.3. an interface to convey the identifiers and the associated values from *the central database*.

12.4. Yamagishi appears to teach a central database accessible by one or more users *(page 13.2.1, figure 1, and pages 13.2.2 and 13.2.3, section 2.2 Database FALNET)*.

12.5. The art of Panchul and the art of Yamagishi are analogous art because they are both directed to a hardware design system.

12.6. The motivation to use the art of Yamagishi with the art of Panchul would have been obvious given the statement in Yamagishi that the database allows much closer integration among tools than other commercially available frameworks *(page 13.2.3, left-side of page, lines 1 – 3)*, which would have been recognized as a benefit by the ordinary artisan.

12.7. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Yamagishi with the art of Panchul to produce the claimed invention.

13. **Examiner's Note:** Examiner has cited particular columns and line numbers in the references applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in their entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

Conclusion

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Russ Guill whose telephone number is 571-272-7955. The examiner can normally be reached on Monday – Friday 9:30 AM – 6:30 PM.
15. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez can be reached on 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Any inquiry of a general nature or relating to the status of this application should be directed to the TC2100 Group Receptionist: 571-272-2100.
16. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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